XS28EGxGE0H3xx

8/16GB eMMC (x8) 3.3V/1.8V FBGA153Balls

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REVISION HISTORY

Revision #	History	Draft Date	Note
0.5	Initial Release	2025-06-24	

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1 Product Overview

1.1 Product Description

The XSemitron's eMMC, which includes both 2D MLC NAND flash and XSEMITRON's in-house controller, is a high-performance

embedded MMC solution designed for various embedded applications. It supports JEDEC eMMC 5.1 version, Command Queue, Enhanced Strobe in HS400, Cache Barrier, Background Operation Control and so on.

A single 3.3V supply voltage is enough for the NAND area (V_{CC}) with internal LDO and 1.8V or 3.3V dual supply voltages (V_{CCQ}) from host is for eMMC controller. Customers are easy to use eMMC in that they don't need to consider any changes inside devices such as flash and thus, it will lead to easier & faster development of applications, ie, better way to the market on time.

THE XSemitron's featured embedded flash management software or FTL(Flash Transition Layer) of eMMC manages high reliability with noticeable Wear Leveling, Bad Block Management and strong ECC. Again, it achieves high performance.

1.2 Product List

XS - 28E - G - 07G – E0 – H3 - E - C - G - A

1 2 3 4 5 6 7 8 9 10

1. **XSemitron**
2. **eMMC**
3. **G: 3.3V + 1.8V**
4. **08G=08GByte**
5. **Internal product version**
6. **Internal product version**
7. **E: 153-ball FBGA, 11.5x13x1.0mm**
8. **C: -25C to + 85C**
9. **G=Green/RoHS/Reach**
10. **Packing Option, A = Tray**

Table 1. Product List

Part No.	Density	BUS	NAND Flash Type	Voltage	Package	Temp.
XS28EG08GE0H3ECGA	8GB	X8	1 Stack	3.3V/1.8V	FBGA153 11.5x13x1.0mm	-25-85℃
XS28EG16GE0H3ECGA	16GB	X8	2 Stack	3.3V/1.8V	FBGA153 11.5x13x1.0mm	-25-85℃

1.3 Key Features

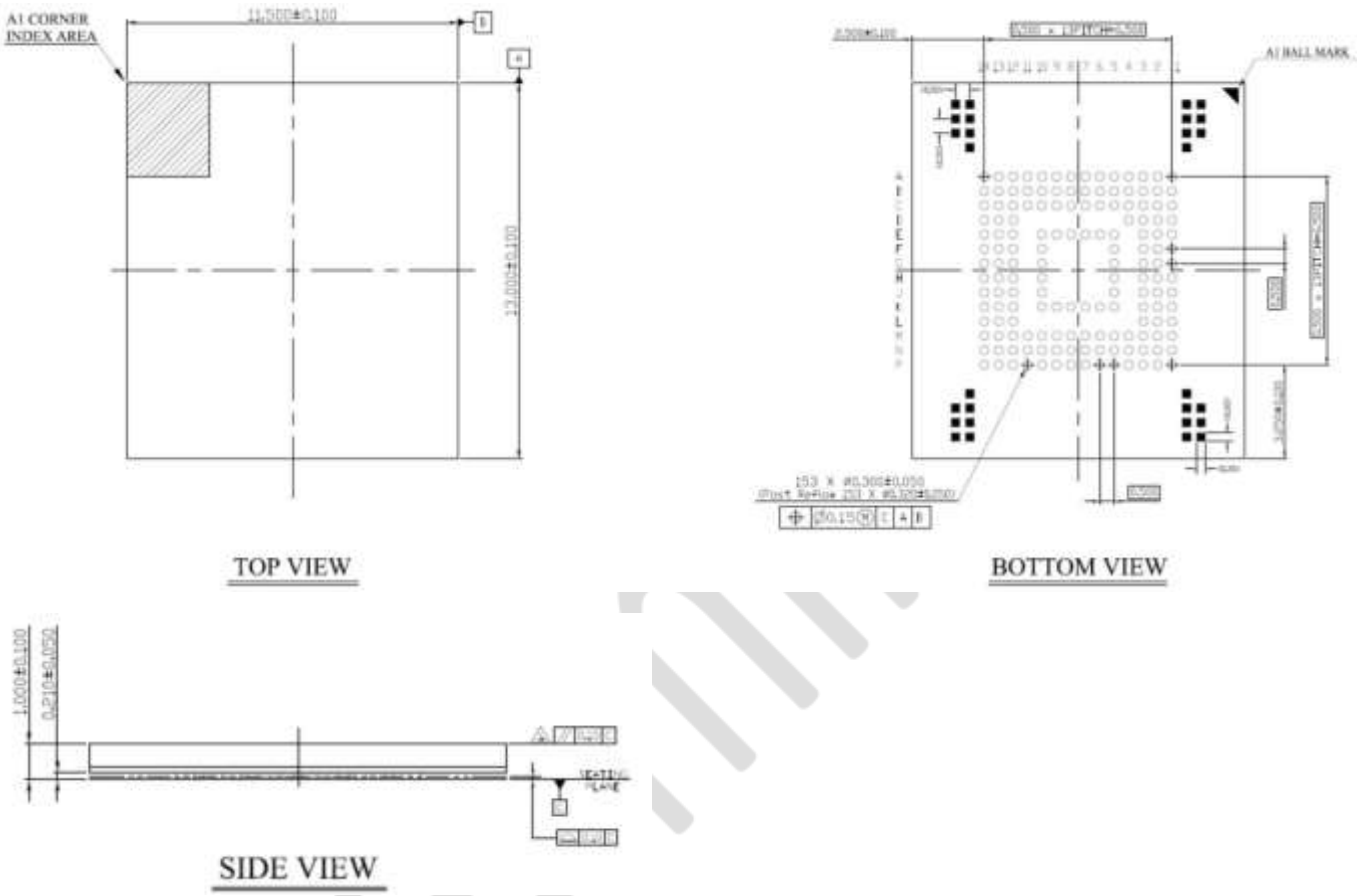
- Supports features of eMMC5.1 which are defined in JEDEC Standard
  - Supported Features: HS400, Field Firmware Update, Security Removal type, Device Health Report
  - Supports CMD Queueing, RPMB Throughput improvement, BKOP Control, Enhanced Strobe, Cache Flushing report, Cache Barrier, and Secure Write Protection of new eMMC standard of version 5.1.
  - Non-supported Features: Large Sector Size (4KB)
- Programmable bus width: 1bit (Default), 4bit, and 8bit Data bus.
- MMC I/F Clock Frequency: 0 ~ 200MHz

  MMC I/F Boot Frequency: 0 ~ 52MHz
- Temperature:
  - Operation -25~85℃, Tc Max = 90 ℃
  - Storage without operation -40~85 ℃

2 Package Information

2.1 Package Dimension

Figure 1. 11.5 x 13.0 x 1.1 (mm) Package Dimension



2.2 Ball & Signal Assignment

Figure 2. eMMC Package Ball Assignment

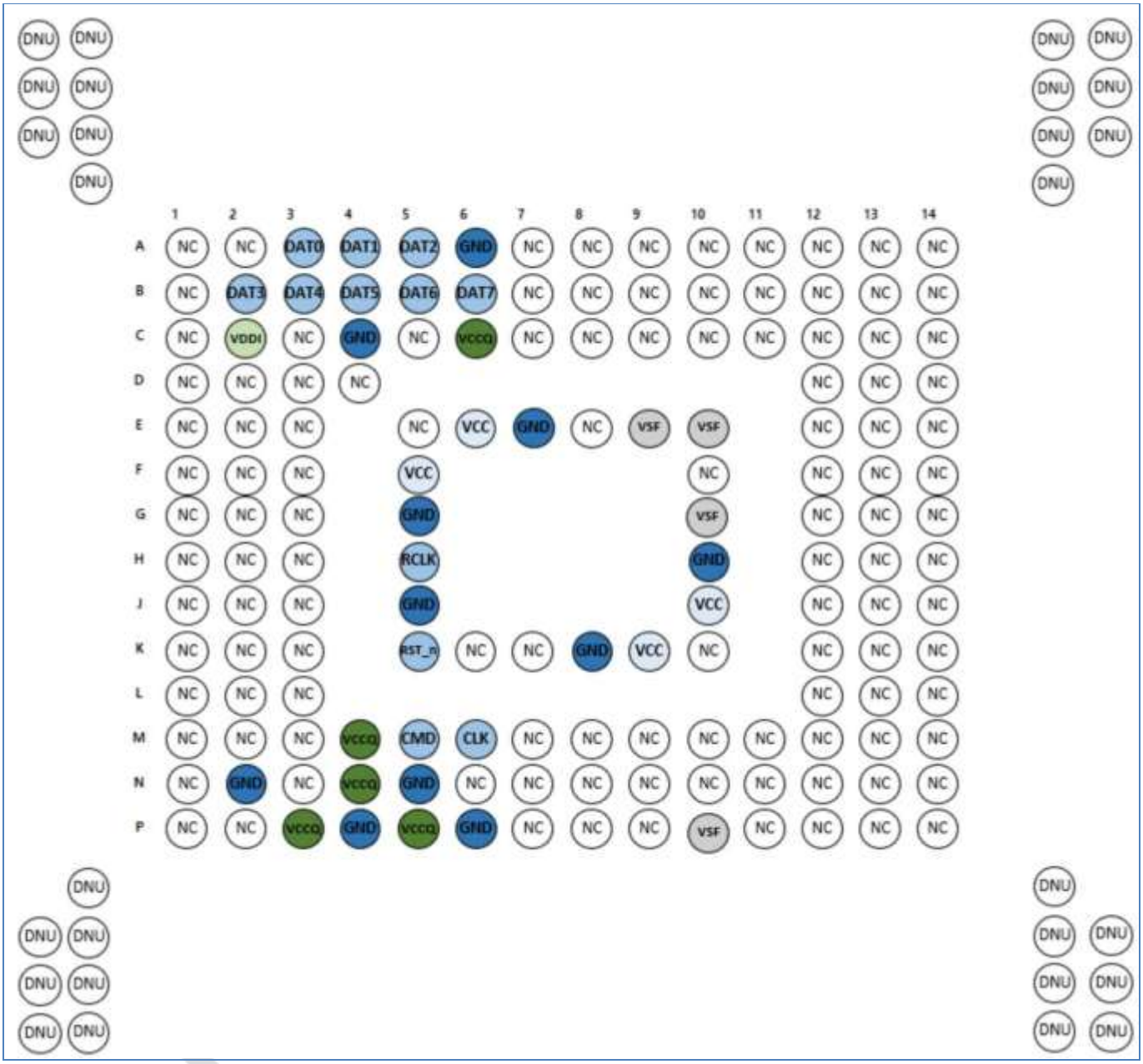


Table 2. Ball & Signal Assignment

No	Signal	Type	Description
A3	DAT0	I/O	Bidirectional channel used for data transfer
A4	DAT1		
A5	DAT2		
B2	DAT3		
B3	DAT4		
B4	DAT5		
B5	DAT6		
B6	DAT7		
M5	CMD	I/O	Command: A bidirectional channel used for device initialization and command transfers. Command operates in two modes, open-drain for initialization and push-pull for fast command transfer.
M6	CLK	I	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines
K5	RSTN		Hardware reset signal pin
H5	Data Strobe	O	Data Strobe : Supports Enhanced strobe of eMMC ver. 5.1
E6	V_{CC}	P	Flash I/O and memory power supply
F5	V_{CC}		
J10	V_{CC}		
K9	V_{CC}		
C6	V_{CCQ}	P	Memory controller core and MMC I/F I/O power supply
M4	V_{CCQ}		
N4	V_{CCQ}		
P3	V_{CCQ}		
P5	V_{CCQ}		
E7	V_{SS}	P	Flash I/O and memory ground connection
G5	V_{SS}		
H10	V_{SS}		
K8	V_{SS}		
A6	V_{SS}		
J5	V_{SS}		
C4	V_{SSQ}	P	Memory controller core and MMC I/F ground connection
N2	V_{SSQ}		
N5	V_{SSQ}		
P4	V_{SSQ}		
P6	V_{SSQ}		
C2	V_{DDi}	P	Internal power node. Connect 0.1uF capacitor from VDDi to ground
E9	VSF		VSF : Vendor Specific Function (For Debug)
E10			
G10			
P10			

NOTE

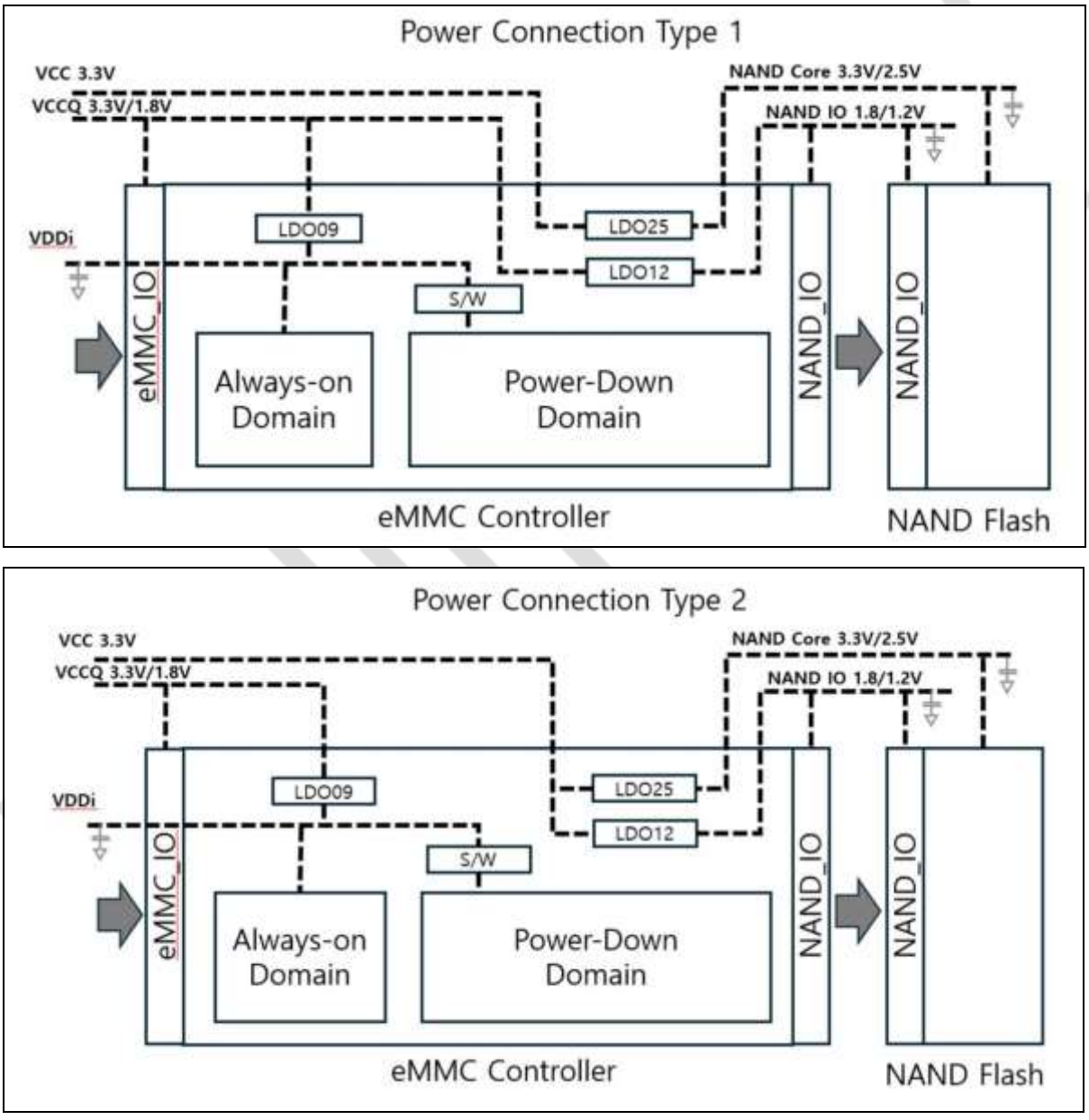
: I/O = Bi-direction, I = Input, O = Output, P = Power/Analog

3 Product Architecture

eMMC consists of NAND flash and controller. V_{CCQ} is for controller power and V_{CC} is for flash power

In the eMMC, V_{CC} is used for the memory device; V_{CCQ} is for the controller and the eMMC interface voltage. Either V_{CC} or V_{CCQ} is for memory interface voltage shown in Figure 3. The core regulator is optional and only required when internal core logic voltage is regulated from V_{CCQ}. A Creg capacitor must be connected to the VDDi terminal to stabilize regulator output on the system.

Figure 3. eMMC Diagram



4 Features

4.1 HS400 Interface

Support HS400 DDR interface timing mode to achieve a bus speed of 400 MB/s at 200MHz clock frequency with 8bit bus width only and the 1.7 ~ 1.95 V_{CCQ} option. At this mode, the host may need to have an adjustable sampling point to reliably receive the incoming data, due to the speed. Please refer to the Bus Timing in Chapter 7.2 for additional information.

4.2 Partitions

The device initially consists of two Boot partitions, RPMB partition, and User Data Area.

Please refer to the table below for Boot partition and RPMB partition size.

Table 3. Boot Area and RPMB Area Partition size

Devices	Partition	Size	Remark
8GB	BOOT1	8,192 KiB	Refer to EXT_CSD[226]
	BOOT2	8,192 KiB	
16GB	BOOT1	16,384 KiB	
	BOOT2	16,384 KiB	
8, 16GB	RPMB	4,096 KiB	Refer to EXT_CSD[168]

Please refer to the table below for User Area partition size.

Table 4. User Density Size

Devices	Max LBA	Size	
8 GB	0x00E9_0000	7,456 MiB	7,818,182,656 Bytes
16 GB	0x01D5_A000	15,028 MiB	15,758,000,128 Bytes

For Enhanced user area, users can configure the related EXT_CSD registers, which has no big impact on device operation.

4.3 Boot operation

Device supports not only boot mode but also alternative boot mode. Device supports high speed timing and dual data rate during boot.

Figure 4. embedded MultiMediaCard state diagram (boot mode)

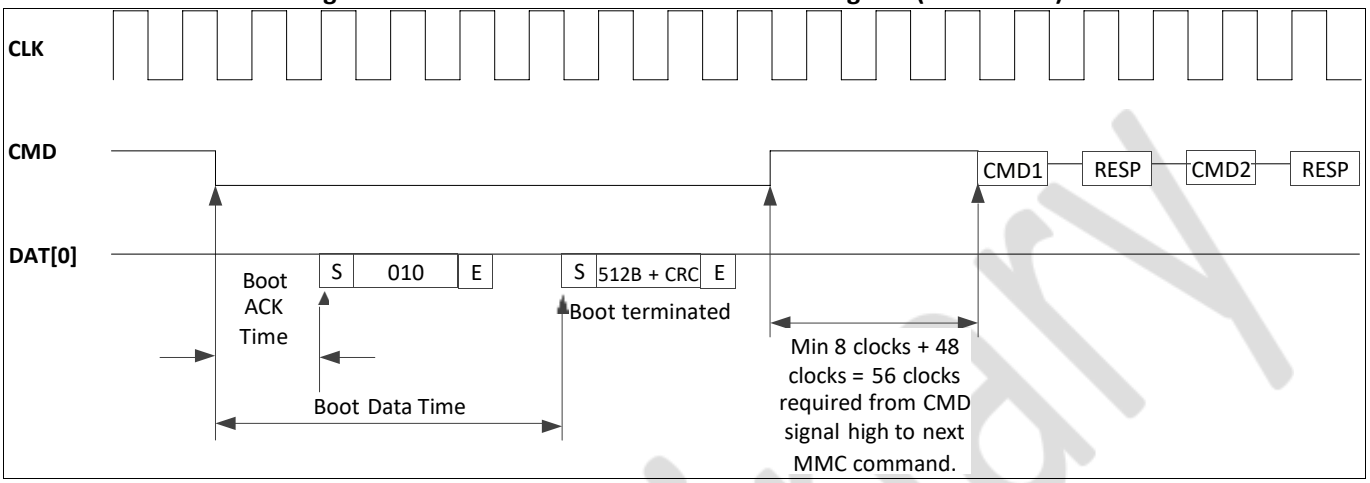


Figure 5. embedded MultiMediaCard state diagram (alternative boot mode)

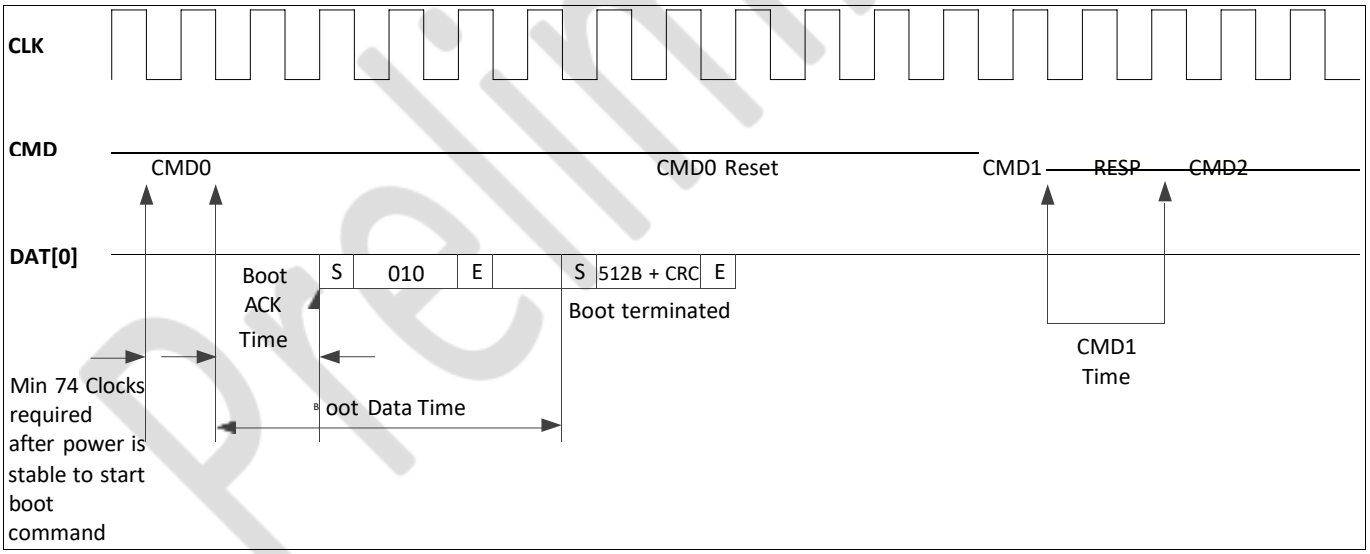


Table 5. Boot ack, boot data and initialization Time

Timing Factor	Value	Remarks
(1) Boot ACK Time	< 10 ms	
(2) Boot Data Time	< 30 ms	

4.4 Cache

eMMC supports volatile SRAM memory as an eMMC cache for performance improvement of both sequential and random access.

4.5 Packed Commands

eMMC supports packed commands feature of eMMC standard version 5.0 and allows the host to pack Read or Write commands into groups (of single type of operation) and transfer these to the device in a single transfer on the bus, which leads to reducing overall bus overheads and thus enables optimal system performance.

4.6 Secure Delete

4.6.1 Sanitize

eMMC supports Sanitize operation for removing data from the unmapped user address space in the device, physically. Device keeps the sanitize operation until one of the following events occurs, with keeping busy asserted,

- Sanitize operation is complete
- HPI is used to abort the operation
- Power failure
- Hardware reset

No data should exist in the unmapped host address space after the sanitize operation is completed.

4.6.2 Secure Erase

eMMC supports the optional Secure Erase command, which is for backward compatibility reasons, as well as standard erase command. Hosts will erase the provided range of LBAs and ensure no older copies of this data exist in the flash with this command.

4.6.3 Secure Trim

eMMC supports Secure Trim command which is like the Secure Erase command but different in that performs a secure purge operation on write blocks instead of erase groups. This is for backward compatibility reasons.
The secure trim command is performed in two steps:

1) Mark targeted LBA range for erase operation.
2) Do Erase the marked address range and then, ensure no old copies are left within that range.

4.7 High Priority Interrupt (HPI)

eMMC supports High Priority Interrupt and prevents a problem of Host being stalled due to too much delayed Write operation by new paging request of operating system, by user. It will delay the request for new paging until currently going write operation is completed.

4.8 Auto Power Saving Mode

eMMC supports Auto Power Saving Mode which can save power consumption definitely. Device will enter this mode if host does not issue any command during 10 ~ 100ms, after completion of a previously issued command.
Any newly issued commands during this mode will be carried normally.

Table 6. Auto Power Saving Mode enter and exit

Mode	Enter Condition	Escape Condition
Auto Power Saving Mode	When a previous operation which came from Host is completed and no command is issued, (1) during 10ms, if there is no cached write data. (2) during 100ms, if there are cached write data.	If Host issues any command

Table 7. Auto Power Saving Mode and Sleep Mode

	Auto Power Saving Mode	Sleep Mode
NAND Power	ON	OFF
Goto Sleep Time	< 10 us, if there is no cached write data. < 2500 us, if there is cached write data.	
Wake Up Time	< 150 us	< 1500 us

4.9 Field Firmware Update (FFU)

Field Firmware Updates (FFU) enables features enhancement in the field. Using this mechanism the host downloads a new version of the firmware to the eMMC device and, following a successful download, instructs the eMMC device to install the new downloaded firmware into the device.

Table 8. FFU Command Sequence

No.	Sequence	Command		Remark
		Index	Argument	
1	Set to Trans state	.....		
2	Set Block Length 512B	16	0x0000_0200	
3	Enter FFU mode	6	0x031E_0100	
4	Send FFU binary	23	0x0000_0200	(1) Sending CMD25 is followed by Sending FFU binary data with FFU_ARG – EXT_CSD[490:487]
5	to Device (Download)	25	0x0000_0000	(2) It's able to send FFU binary data to a Open-ended Write.
6	Check FFU result	8	0x0000_0000	Check FFU_STATUS - EXT_CSD[26] If 0, FFU is success, Otherwise, FFU is fail.
7	Exit FFU mode	6	0x031E_0000	
8	CMD0 / HW Reset / Power Reset	Full FW programmed to NAND will be loaded.		
9	Re-Init to Trans state	CMD0, CMD1, ...		

5 Performance

Table 9. Sustained Sequential Performance

Devices	Sequential Read (MB/s)	Sequential Write (MB/s)	Random Read (IOPS)	Random Write (IOPS)
8 GB	250	30	16,000	18,000
16 GB	290	60	21,000	20,000

- Precondition: Clean & Sustained
- Test condition: Bus width x8, HS400, 512KB data transfer, Command Queue On, Cache On, w/o file system overhead, measured on The XSemitron's internal board and scenarios.

6 Register Value

The following sections are for describing all register value of eMMC device at its default in the eMMC. And these values here may be updated in a later version without notice.

There are defined total six registers in this section: OCR, CID, CSD, EXT_CSD, RCA and DSR. All of them have its own commands corresponded and for details. The OCR, CID and CSD registers have information of device and content, while the RCA and DSR registers are for configuring parameters of devices. For the EXT_CSD register, it contains both device specific information and actual configuration parameters.

6.1 OCR Register

The operation conditions register (OCR) contains: V_{CC} voltage profile of the device, access mode indication, status information bit. The status bit is set when the device finishes its power up procedure.

All eMMC devices shall have this register implemented.

Table 10. OCR Register

OCR bit	V_{CCQ} Voltage Window	Register Value
[6:0]	Reserved	00 00000b
[7]	1.70 ~ 1.95	1b
[14:8]	2.0 ~ 2.6	000 0000b
[23:15]	2.7 ~ 3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	00b (byte mode) -[2GB] 10b (sector mode) -[*Higher than 2GB only]
[31]	eMMC power up status bit (busy)[1]	

NOTE

1) This bit is set to LOW during the busy power up routine.
2) The voltage for internal flash memory(V_{CC}) should be 2.7 ~ 3.6V regardless of OCR register value.

6.2 CID Register

The device Identification (CID) register is 128bits wide and it contains the device identification information used during the device identification phase (eMMC protocol). eMMC devices shall have a unique identification number.

Users can define their own CID register, and the CID contents will be programmed into the eMMC device during firmware down-loading process. Once programming is complete, then end users cannot change CID unless the whole foundry production program is re-done again. And users can install the new downloaded firmware into the device by using FFU (Field Firmware Update) mode.

Table 11. CID Register

Name	Field	Width	CID-slice	CID Value
Manufacturer ID	MID	8	[127:120]	0xEE
Reserved		6	[119:114]	00 00000b
Device/BGA	CBX	2	[113:112]	0x01
OEM/Application ID	OID	8	[111:104]	0x0A
Product name	PNM	48	[103:56]	Refer to chapter 6.2.1
Product revision	PRV	8	[55:48]	0x00
Product serial number	PSN	32	[47:16]	TBD

Manufacturing date	MDT	8	[15:8]	TBD
CRC7 checksum	CRC	7	[7:1]	---
not used, always ,1,	-	1	[0:0]	---

6.2.1 Product name table (In CID Register)

The product name, PNM, is a string, 6 ASCII characters long.

Table 12. Product name table

Part Number	Devices	Product Name in CID Register (PNM)
XS28EG08GE0H3ECGA	8 GB	E12HBS
XS28EG16GE0H3ECGA	16 GB	E13HBD

6.3 RCA Register

The writable 16-bit relative device address (RCA) register carries the device address assigned by the host during the device identification. This address is used for the addressed host-device communication after the device identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all devices into the Stand-by State with CMD7.

6.4 CSD Register

The device Specific Data (CSD) register provides information on how to access the device contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E) can be changed by CMD27.

The CSD register defines the behavior of eMMC devices. The eMMC behavior is related to controller design. The following table shows a typical CSD definition of eMMC based eMMC. If users need to add on more features, firmware or hardware modifications may be necessary.

※ Note that the register values are preliminary data and may be updated in a later version. And the updated value will be supported by specified application note later.

Table 13. eMMC Typical CSD Register

Name	Field	Bit	Type	Slice	Value	Note
CSD structure	CSD_STRUCTURE	2	R	[127:126]	0x03	
System specification version	SPEC_VERS	4	R	[125:122]	0x04	
Reserved	-	2	R	[121:120]	-	
Data read access-time 1	TAAC	8	R	[119:112]	0x27	
Data read access-time 2 in CLK cycles (NSAC x 100)	NSAC	8	R	[111:104]	0x01	
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	0x32	
Device command classes	CCC	12	R	[95:84]	0x8F5	
Max. read data block length	READ_BL_LEN	4	R	[83:80]	0x09	
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0x00	
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0x00	
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0x00	
DSR implemented	DSR_IMP	1	R	[76:76]	0x00	
Reserved	-	2	R	[75:74]	-	
Device size	C_SIZE	12	R	[73:62]	0xFFF	
Max read current@VCCQ min	VCCQ_R_CURR_MIN	3	R	[61:59]	0x07	
Max read current@VCCQ max	VCCQ_R_CURR_MAX	3	R	[58:56]	0x07	
Max write current@VCCQ min	VCCQ_W_CURR_MIN	3	R	[55:53]	0x07	
Max write current@VCCQ max	VCCQ_W_CURR_MAX	3	R	[52:50]	0x07	
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	0x07	
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	0x1F	
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	0x1F	
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0x0F	
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	0x01	
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0x00	
Write speed factor	R2W_FACTOR	3	R	[28:26]	0x02	
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	0x09	

Name	Field	Bit	Type	Slice	Value	Note
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0x00	
Reserved	-	4	R	[20:17]	-	
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0x00	
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0x00	
Copy flag (OTP)	COPY	1	R/W	[14:14]	0x01	
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0x00	
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0x00	
File format	FILE_FORMAT	2	R/W	[11:10]	0x00	
ECC code	ECC	2	R/W/E	[9:8]	0x00	
CRC	CRC	7	R/W/E	[7:1]	-	
Not used, always '1,	-	1	-	[0:0]	-	
Not used, always '1,	-	1	-	[0:0]	-	

NOTE

: The following is for the type of the CSD Register entries in theTable 143.

R: Read only

W: One time programmable and not readable

R/W: One time programmable and readable

W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.

R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.

R/W/C_P: Writable after value cleared by power failure and HW/rest assertion (the value not cleared by CMD0 reset) and readable.

R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.

W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

6.5 Extended CSD Register (EXT_CSD)

The Extended CSD register defines the additional behavior of eMMC devices due to limited CSD information. The following table shows a typical extended CSD definition of eMMC. If users need to add on more features, firmware or hardware modifications may be necessary.

※ Note that the register values are preliminary data and may be updated in a later version. And the updated value will be supported by specified application note later.

Table 14. eMMC Typical EXT_CSD Register

Name	Field	Byte	Type	Slice	Value	Note
Properties Segment						
Reserved	-	6	-	[511:506]	-	
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	0x00	
Supported command sets	S_CMD_SET	1	R	[504]	0x01	
HPI features	HPI_FEATURES	1	R	[503]	0x01	
Background operations Support	BKOPS_SUPPORT	1	R	[502]	0x01	
Max packed read commands	MAX_PACKED_READS	1	R	[501]	0x3F	
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	0x3F	
Data tag support	DATA_TAG_SUPPORT	1	R	[499]	0x01	
Tag unit size	TAG_UNIT_SIZE	1	R	[498]	0x08	128KB
Tag resources size	TAG_RES_SIZE	1	R	[497]	0x00	
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	0x05	
Large unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0x07	
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	0x03	
Supported modes	SUPPORTED_MODES	1	R	[493]	0x01	
FFU features	FFU_FEATURES	1	R	[492]	0x00	
Operation codes timeout	OPERATION_CODE_ TIMEOUT	1	R	[491]	0x10	6.5536s
FFU Argument	FFU_ARG	4	R	[490:487]	0x00	
Barrier Support	BARRIER_SUPPORT	1	R	[486]	0x01	
Reserved	-	181	-	[485:309]	-	
CMDQ Support	CMDQ_SUPPORT	1	R	[308]	0x01	
CMDQ Depth	CMDQ_DEPTH	1	R	[307]	0x1F	
Reserved	-	1	-	[306]	-	
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTOR S_CORRECTLY_PROGRAM MED	4	R	[305:302]	0x00	
Vendor proprietary health report	VENDOR_PROPRIETARY_ HEALTH_REPORT	32	R	[301:270]	0x00	
Device life time estimation type B	DEVICE_LIFE_TIME_ EST_TYP_B	1	R	[269]	0x01	For User Blocks
Device life time estimation type A	DEVICE_LIFE_TIME_ EST_TYP_A	1	R	[268]	0x01	For Meta Blocks
Pre EOL information	PRE_EOL_INFO	1	R	[267]	0x01	
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	0x00	
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	0x04	
Optimal trim unit size	OPTIMAL_TRIM_	1	R	[264]	0x03	

Name	Field	Byte	Type	Slice	Value	Note
	UNIT_SIZE					
Device version	DEVICE_VERSION	2	R	[263:262]	0x00	
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	→	FW Patch Ver.
Power class for 200MHz, DDR at V_{CC}=3.6V	PWR_CL_DDR_200_360	1	R	[253]	0x77	
Cache size	CACHE_SIZE	4	R	[252:249]	→	0x00000400
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x64	1000 ms
Power off notification(long) timeout	POWER_OFF_ LONG_TIME	1	R	[247]	0x64	1000 ms
Background operations status	BKOPS_STATUS	1	R	[246]	0x00	
Number of correctly programmed sectors	CORRECTLY_PRG_ SECTORS_NUM	4	R	[245:242]	→	0x00000000
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0x1E	3000 ms
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	R	[240]	0x01	
Power class for 52MHz, DDR at V_{CC} = 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x77	
Power class for 52MHz, DDR at V_{CC} = 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0x77	
Power class for 200MHz at V_{CCQ} = 1.95V, V_{CC} = 3.6V	PWR_CL_200_195	1	R	[237]	0x77	
Power class for 200MHz, at V_{CCQ} = 1.3V, V_{CC} = 3.6V	PWR_CL_200_130	1	R	[236]	0x00	
Minimum write performance for 8 bit at 52 MHz in DDR mode	MIN_PERF_ DDR_W_8_52	1	R	[235]	0x00	
Minimum read performance for 8 bit at 52 MHz in DDR mode	MIN_PERF_ DDR_R_8_52	1	R	[234]	0x00	
Reserved	-	1	-	[233]	-	
TRIM multiplier	TRIM_MULT	1	R	[232]	0x03	
Secure feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x55	
Secure erase multiplier	SEC_ERASE_MULT	1	R	[230]	0x0A	
Secure trim multiplier	SEC_TRIM_MULT	1	R	[229]	0x0A	
Boot information	BOOT_INFO	1	R	[228]	0x07	
Reserved	-	1	-	[227]	-	
Boot partition size	BOOT_SIZE_MULTI	1	R	[226]	→	0x40-8GB, 0x80-16GB
Access size	ACC_SIZE	1	R	[225]	0x06	
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	0x01	
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0x03	
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	0x01	
High-capacity write protect	HC_WP_GRP_SIZE	1	R	[221]	→	0x10 for 8, 16GB

Name	Field	Byte	Type	Slice	Value	Note
group size						
Sleep current (V_{CC})	S_C_VCC	1	R	[220]	0x07	
Sleep current (V_{CCQ})	S_C_VCCQ	1	R	[219]	0x07	
Product state awareness timeout	PRODUCTION_STATE_ AWARENESS_TIMEOUT	1	R	[218]	0x0D	1,638.4 ms
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x12	26.2144 ms
Sleep notification timeout	SLEEP_NOTIFICATION_ TIME	1	R	[216]	0x10	1,310.72 ms
Sector count	SEC_COUNT	4	R	[215:212]	→	Refer to chapter 4.2
Secure Write Protect Information	SECURE_WP_INFO	1	R	[211]	0x01	
Minimum write performance for 8bit at 52MHz	MIN_PERF_ W_8_52	1	R	[210]	0x00	
Minimum read performance for 8bit at 52MHz	MIN_PERF_ R_8_52	1	R	[209]	0x00	
Minimum write performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_ W_8_26_4_52	1	R	[208]	0x00	
Minimum read performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_ R_8_26_4_52	1	R	[207]	0x00	
Minimum write performance for 4bit at 26MHz	MIN_PERF_ W_4_26	1	R	[206]	0x00	
Minimum read performance for 4bit at 26MHz	MIN_PERF_ R_4_26	1	R	[205]	0x00	
Reserved	-	1	-	[204]	-	
Power class for 26 MHz at 3.6V 1 R	PWR_CL_26_360	1	R	[203]	0x77	
Power class for 52 MHz at 3.6V 1 R	PWR_CL_52_360	1	R	[202]	0x77	
Power class for 26 MHz at 1.95V 1 R	PWR_CL_26_195	1	R	[201]	0x77	
Power class for 52 MHz at 1.95V 1 R	PWR_CL_52_195	1	R	[200]	0x77	
Partition switching timing	PARTITION_ SWITCH_TIME	1	R	[199]	0x01	10 ms
Out-of-interrupt busy timing	OUT_OF_ INTERRUPT_TIME	1	R	[198]	0x64	1000 ms
I/O Driver Strength CSD	DRIVER_STRENGTH	1	R	[197]	0x1F	
Device type	DEVICE_TYPE	1	R	[196]	0x57	
Reserved	-	1	-	[195]	-	
CSD STRUCTURE	CSD_STRUCTURE	1	R	[194]	0x02	
Reserved	-	1	-	[193]	-	
Extended CSD revision	EXT_CSD_REV	1	R	[192]	0x08	

Name	Field	Byte	Type	Slice	Value	Note
Modes Segment						
Command set	CMD_SET	1	R/W/E_P	[191]	0x00	
Reserved	-	1	-	[190]	-	
Command set revision	CMD_SET_REV	1	R	[189]	0x00	
Reserved	-	1	-	[188]	-	
Power class	POWER_CLASS	1	R/W/E_P	[187]	0x00	
Reserved	-	1	-	[186]	-	
High-speed interface timing	HS_TIMING	1	R/W/E_P	[185]	0x00	
Strobe Support	STROBE_SUPPORT	1	R	[184]	0x01	
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	0x00	
Reserved	-	1	-	[182]	-	
Erased memory content	ERASED_MEM_CONT	1	R	[181]	0x00	
Reserved	-	1	-	[180]	-	
Partition configuration	PARTITION_CONFIG	1	R/W/E & R/W/E_P	[179]	0x00	
Boot config protection	BOOT_CONFIG_PROT	1	R/W & R/W/C_P	[178]	0x00	
Boot bus conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0x00	
Reserved	-	1	-	[176]	-	
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	0x00	
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0x00	
Boot area write protection register	BOOT_WP	1	R/W & R/W/C_P	[173]	0x00	
Reserved	-	1	-	[172]	-	
User area write protection register	USER_WP	1	R/W, R/W/C_P & R/W/E_P	[171]	0x00	
Reserved	-	1	-	[170]	-	
FW configuration	FW_CONFIG	1	R/W	[169]	0x00	
RPMB size	RPMB_SIZE_MULT	1	R	[168]	0x20	
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x1F	
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	0x14	
Start sanitize operation	SANITIZE_START	1	W/E_P	[165]	0x00	
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00	
Enable background operations handshake	BKOPS_EN	1	R/W	[163]	0x00	
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0x00	

Name	Field	Byte	Type	Slice	Value	Note
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x00	
Partitioning support	PARTITIONING_SUPPORT	1	R	[160]	0x07	
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	→	8GB(0x0001D2) 16GB(0x0003AB)
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x00	
Partitioning Setting	PARTITION_SETTING_ COMPLETED	1	R/W	[155]	0x00	
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	0x00	
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	0x00	
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0x00	
Reserved	-	1	-	[135]	-	
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0x00	
Production state awareness	PRODUCTION_ STATE_AWARENESS	1	R/W/E	[133]	0x00	
Package Case Temperature is Controlled	TCASE_SUPPORT	1	W/E_P	[132]	0x00	
Periodic Wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0x00	
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_ DDR_SUPPORT	1	R	[130]	0x01	
Reserved	-	2	-	[129:128]	-	
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64		[127:64]	0x00	
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0x00	
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0x00	
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0x00	
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0x00	
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	0x00	
Number of addressed group to be released	DYNCAP_NEEDED	1	R	[58]	0x00	
Exception events control	EXCEPTION_EVENTS_ CTRL	2	R/W/E_P	[57:56]	0x00	
Exception events status	EXCEPTION_EVENTS_ STATUS	2	R	[55:54]	0x00	
Extended Partitions Attribute	EXT_PARTITIONS_ ATTRIBUTE	2	R/W	[53:52]	0x00	
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0x00	
Packed command status	PACKED_COMMAND_ STATUS	1	R	[36]	0x00	
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0x00	

Name	Field	Byte	Type	Slice	Value	Note
Power Off Notification	POWER_OFF_ NOTIFICATION	1	R/W/E_P	[34]	0x00	
Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	0x00	
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0x00	
Control to Turn the Barrier ON/OFF	BARRIER_CTRL	1	R/W	[31]	0x00	
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0x00	
Mode operation codes	MODE_OPERATION_ CODES	1	W/E_P	[29]	0x00	
Reserved	-	2	-	[28:27]	-	
FFU status	FFU_STATUS	1	R	[26]	0x00	
Pre loading data size	PRE_LOADING_ DATA_SIZE	4	R/W/E_P	[25:22]	→	0x0000_0000
Max pre loading data size	MAX_PRE_LOADING_ DATA_SIZE	4	R	[21:18]	→	8GB(0x003B_0000) 16GB(0x0076_0000)
Product state awareness enablement	PRODUCT_ STATE_AWARENESS_ ENABLEMENT	1	R/W/E & R	[17]	0x03	
Secure Removal type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	0x09	
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0x00	
Reserved	-	15	-	[14:0]	-	

NOTE

: The following is for the type of the EXT_CSD Register entries in theTable 14.

R: Read only.

W: One time programmable and not readable.

R/W: One time programmable and readable.

W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.

R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.

R/W/C_P: Writable after value cleared by power failure and HW/reset assertion (the value not cleared by CMD0 reset) and readable.

R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.

W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

7 AC Parameter

7.1 Timing Parameter

Table 15. Timing Parameter

Timing Paramter		Max. Value
Initialization Time (tINIT)	w/ PON [1)]	50 ms
	wo/ PON [1)]	500 ms
	SPO [1)]	1 sec
	After partition setting [2)]	3 sec
Read Timeout		150 ms
Write Timeout		600 ms
Erase Timeout		900 ms
Force Erase Timeout		3 min
Secure Erase Timeout		9 sec
Secure Trim Timeout		9 sec
Trim Timeout		900 ms
Partition Switching Timeout (after Init)		10 ms
Power Off Notification (Short) Timeout		1 sec
Power Off Notification (Long) Timeout		1 sec

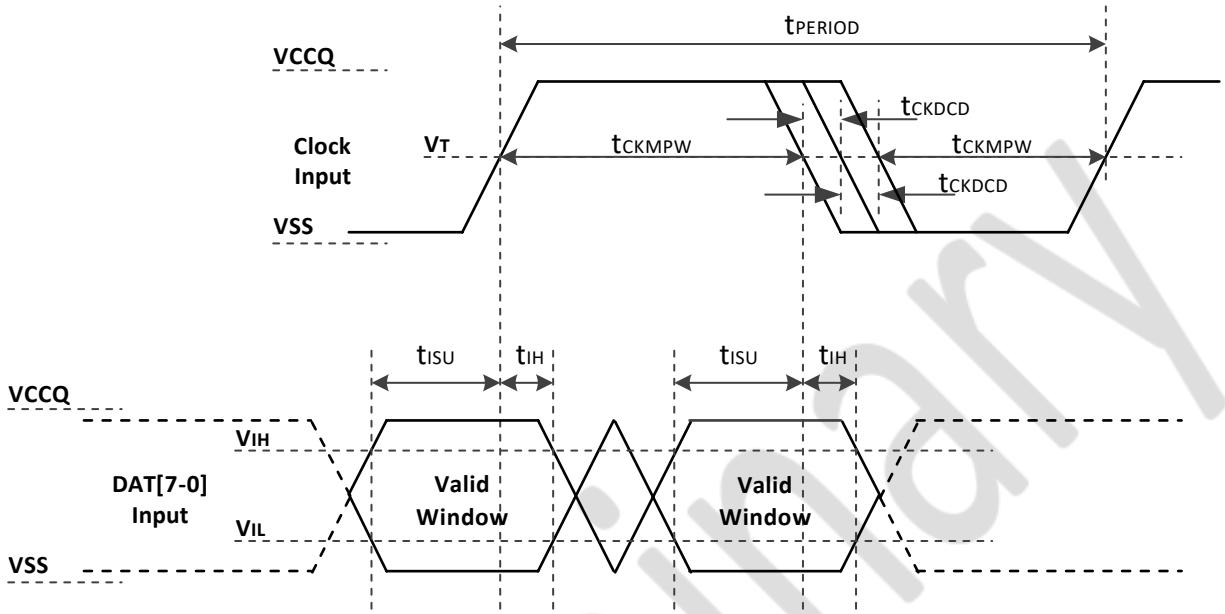
NOTE

1) Initialization Time without partition setting.
2) For the Initialization Time after partition setting, refer to INI_TIMEOUT_AP in 6.4 EXT_CSD register.
3) All those Timeout Values specified in the above Table are only for testing purposes under specific test case only and they can vary in real cases. Also, it may be affected may vary due to user environment.

7.2 Bus Timing Specification in HS400 mode

7.2.1 HS400 Device Input Timing

Figure 6. HS400 Device Input Timing Diagram



NOTE

1) t_{ISU} and t_{IH} are measured at V_{IL} (max) and V_{IH} (min).
2) V_{IH} denotes V_{IH} (min) and V_{IL} denotes V_{IL} (max)

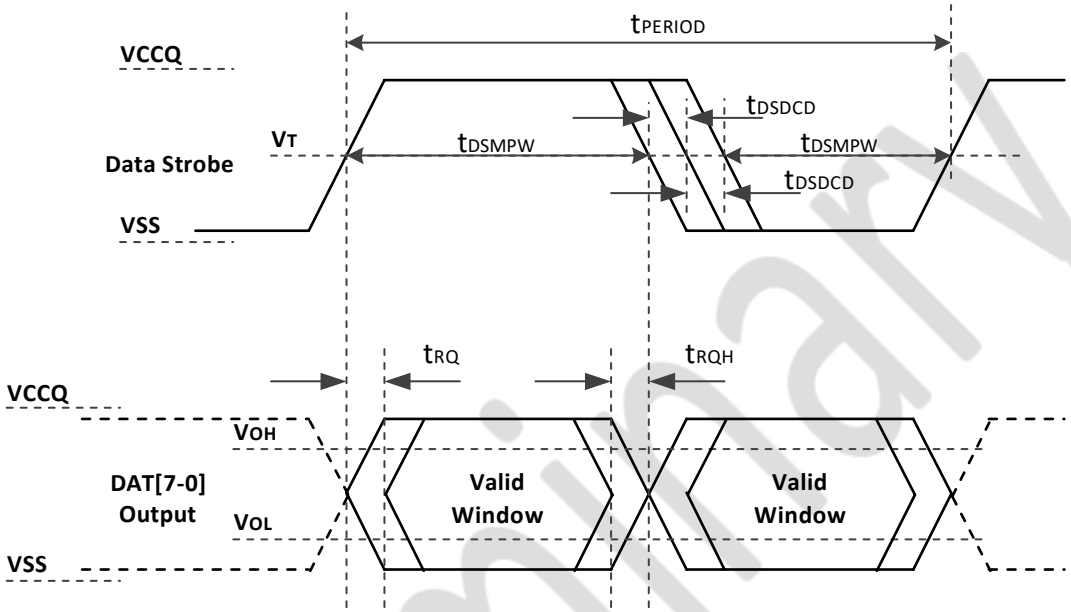
Table 16. HS400 Device Input Timing

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK					
Cycle time data transfer mode	t_{PERIOD}	5	-	ns	200MHz(Max), between rising edges with respect to V_T.
Slew rate	SR	1.125	-	V/ns	
Duty cycle distortion	t_{CKDCD}	0.0	0.3	ns	
Minimum pulse width	t_{CKMPW}	2.2	-	ns	
Input DAT (referenced to CLK)					
Input set-up time	t_{ISUddr}	0.4	-	ns	
Input hold time	t_{IHddr}	0.4	-	ns	
Slew rate	SR	1.125	-	V/ns	

7.2.2 HS400 Device Output Timing

Data Strobe is used to read data (data read and CRC status response read) in HS400 mode. The device output value of Data Strobe is “High-Z” when the device is not sending data (data read, CRC status response). Data Strobe is toggled only during data read period.

Figure 7. HS400 Device Output Timing Diagram



NOTE

1) V_{OH} denotes V_{OH} (min) and V_{OL} denotes V_{OL} (max).

Table 17. HS400 Device Output Timing

Parameter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time data transfer mode	t_{PERIOD}	5	-	ns	200MHz(max), between rising edges with respect to V_T.
Slew rate	SR	1.125	-	V/ns	
Duty cycle distortion	t_{DSDCD}	0.0	0.2	ns	
Minimum pulse width	t_{DSMPW}	2.0	-	ns	
Read pre-amble	t_{RPRE}	0.4	-	t_{PERIOD}	
Read post-amble	t_{RPST}	0.4	-	t_{PERIOD}	
Output DAT (referenced to Data Strobe)					
Output skew	t_{RQ}	-	0.4	ns	
Output hold skew	t_{RQH}	-	0.4	ns	
Slew rate	SR	1.125	-	V/ns	

7.3 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

Figure 8. Bus Signal Levels

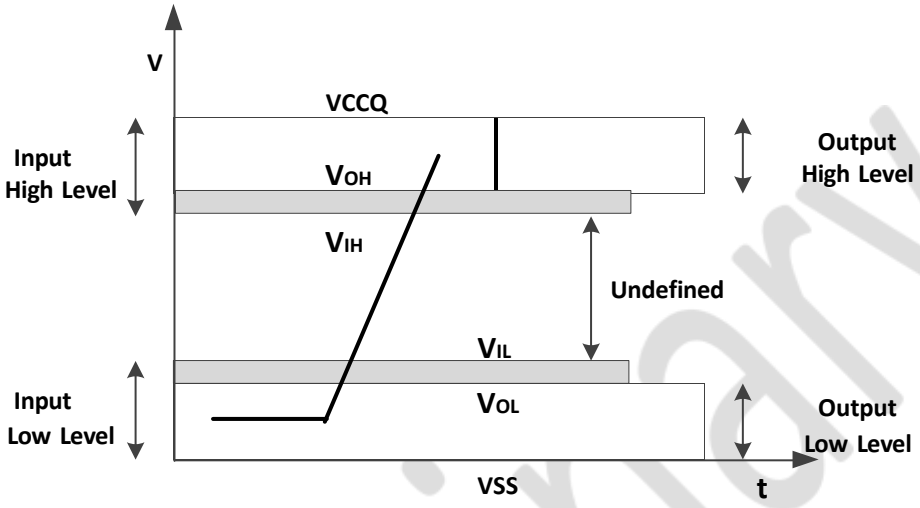


Table 18. Bus Signal Levels

Parameter	Symbol	Min	Max	Unit	Remark
Open-drain mode					
Output HIGH voltage	V_{OH}	V_{CCQ} - 0.2	-	V	-
Output LOW voltage	V_{OL}	-	0.3	V	I_{OL} = 2mA
Push-pull mode (High-voltage eMMC)					
Output HIGH voltage	V_{OH}	0.75 x V_{CCQ}	-	V	I_{OH} = -100uA @ V_{CCQ} min
Output LOW voltage	V_{OL}	-	0.125 x V_{CCQ}	V	I_{OL} = 100uA @ V_{CCQ} min
Input HIGH voltage	V_{IH}	0.625 x V_{CCQ}	V_{CCQ} + 0.3	V	-
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.25 x V_{CCQ}	V	-
Push-pull mode (1.70 ~ 1.95 V)					
Output HIGH voltage	V_{OH}	V_{CCQ} - 0.45	-	V	I_{OH} = -2mA
Output LOW voltage	V_{OL}	-	0.45	V	I_{OL} = 2mA
Input HIGH voltage	V_{IH}	0.65 x V_{CCQ} [1)]	V_{CCQ} + 0.3	V	-
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.35 x V_{CCQ} [2)]	V	-

NOTE

1) Because V_{OH} depends on external resistance value (including outside the package), this value does not apply to device specification. The host is responsible for choosing the external pull-up and open drain resistance value to meet V_{OH} Min value.

2) 0.7 x V_{CCQ} for MMC4.3 and older revisions.

3) 0.3 x V_{CCQ} for MMC4.3 and older revisions.

8 DC Parameter

8.1 Power Consumption

Table 19. Active Power Consumption during operation

Density (GB)	NAND	CTRL (mA)	NAND (mA)
8	2D MLC 64Gb x 1	95	130
16	2D MLC 64Gb x 2	95	140

NOTE

* Power Measurement conditions: Bus configuration =x8 @200MHz DDR

* The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

Table 20. Standby Power Consumption in auto power saving mode and standby state

Density (GB)	NAND	CTRL (uA)		NAND (uA)	
		25°C	85°C	25°C	85°C
8	2D MLC 64Gb x 1	200	1200	25	30
16	2D MLC 64Gbx 2	200	1200	40	50

NOTE

* Power Measurement conditions: Bus configuration =x8, No CLK

* No background operation (ex. Patrol Read)

Table 21. Sleep Power Consumption in Sleep State

Density (GB)	NAND	CTRL (uA)		NAND (uA)
		25°C	85°C	
8	2D MLC 64Gb x 1	200	1200	0[1)]
16	2D MLC 64Gb x 2	200	1200	

NOTE

* Power Measurement conditions: Bus configuration =x8, No CLK

*1) In sleep mode NAND power can be turned off.

If NAND power is alive, NAND power is equal to that of the Standby state.

8.2 Supply Voltage

Table 22. Supply Voltage

Symbol	Min (V)	Max (V)
V_{CCQ} (Low)	1.7	1.95
V_{CCQ} (High)	2.7	3.6
V_{CC}	2.7	3.6

8.3 Bus Signal Line Load

The total capacitance CL of each line of the eMMC bus is the sum of the bus master capacitance CHOST, the bus capacitance CBUS itself and the capacitance CDEVICE of the eMMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances should be under 20pF.

Table 23. Bus Signal Line Load

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100	KOhm	to prevent bus floating
Pull-up resistance for DAT0-DAT7	R_{DAT}	10		100	KOhm	to prevent bus floating
Internal pull up resistance DAT1-DAT7	R_{int}	10		150	KOhm	to prevent unconnected lines floating
Single Device capacitance	C_{DEVICE}			6	pF	
Maximum signal line inductance				16	nH	f_{PP} <= 52 MHz

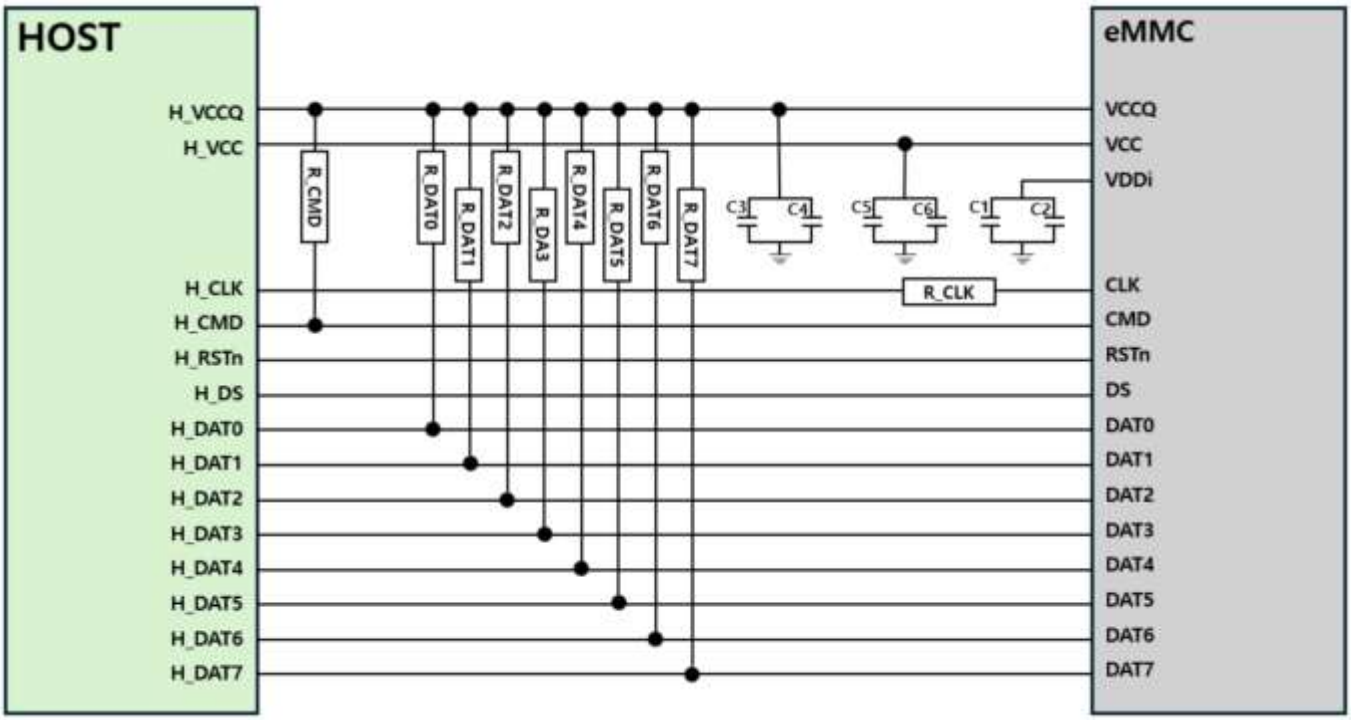
Table 24. Capacitance and Resistance for HS400 mode

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Bus signal line capacitance	C_L			13	pF	Single Device
Single Device capacitance	C_{DEVICE}			6	pF	
Pull-down resistance for Data Strobe	$R_{Data\ Strobe}$	10		100	KOhm	Optional

9 Capacitor Specifications

9.1 Capacitor Connection Guidelines

Figure 9. Connection guide drawing



Parameter	Symbol	Min	Max	Unit	Comment
VDDI	C1 + C2	0.1	4.7	uF	If the target device bus speed mode is either backward-compatible, high speed SDR, high speed DDR, or HS200, Min value is 0.1uF If the target device bus speed mode is HS400, Min value is 1uF
VCCQ	C3 + C4	1	4.7	uF	
VCC	C5 + C6	1	10	uF	

Note

Coupling capacitor should be connected with VDD and VSS as closely as possible.

Capacitor Types are as follows:

- SMT-Ceramic
- X5R/X7R
- 6.3V/10V
- Min height - 0.55mm
- Foot Print: 0402 or above

Capacitors should be located as close to the supply ball as possible and they will eliminate as many trace inductance effects as possible and give a cleaner voltage supply to the device. Also, they reduce lead length and eliminate noise coupling onto through-hole components, which may have antenna effects.